**LAB NO 11**



**Fall 2024**

**CSE-304L Computer Organization and Architecture Lab**

Submitted by:

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Reg no**. : 22PWCSE2144**

ClassSection **: A**

Signature: \_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

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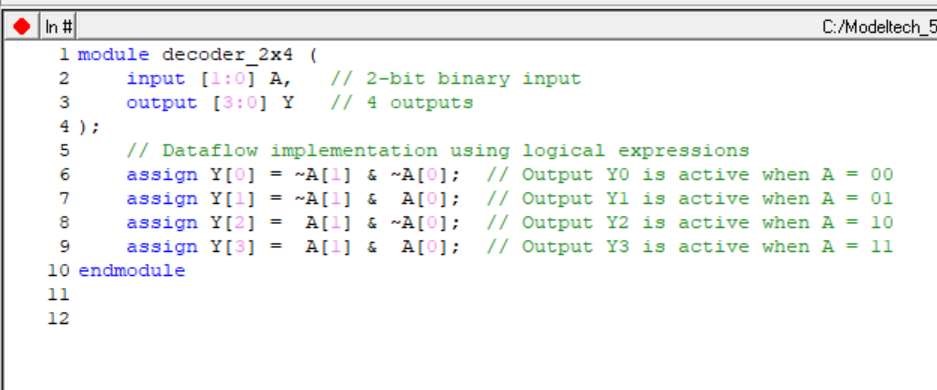
**Decoder:**

TASK1:

Write a Verilog code for 2x4 Decoder using Dataflow Level modeling.

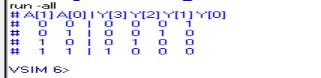
CODE:

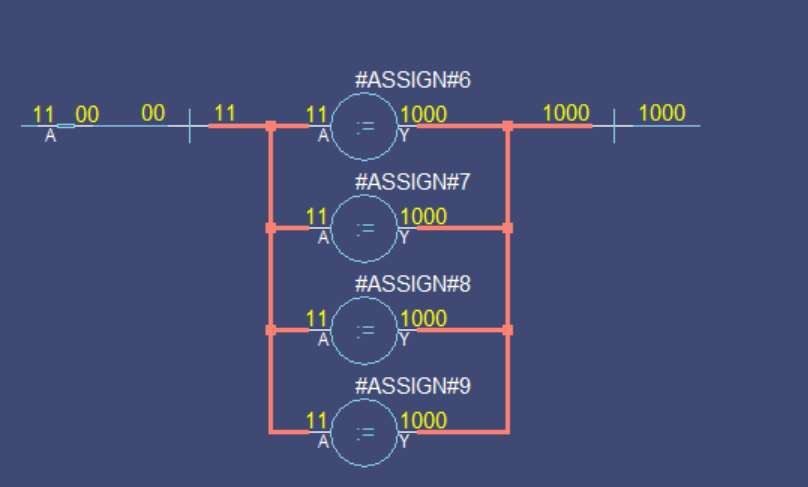
A screenshot of a computer program

Description automatically generated

Output:

**Table:**

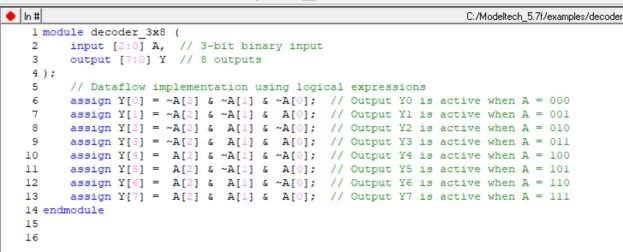


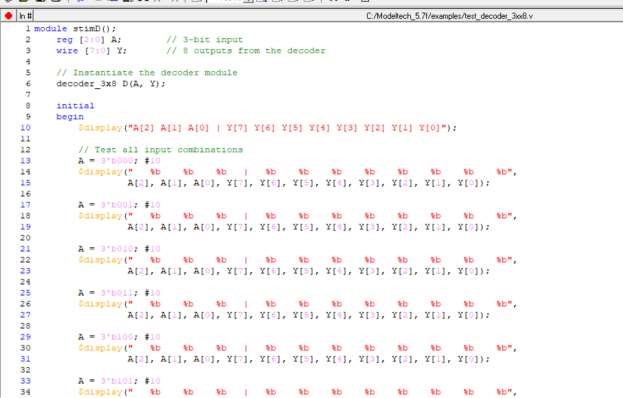


**Task 2:**

Write a Verilog code for 3x8 Decoder using Dataflow Level modeling.

**Code:**

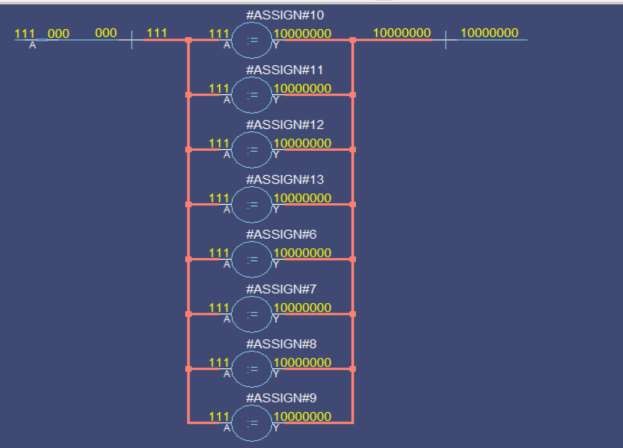




**Table output:**

A screenshot of a computer code

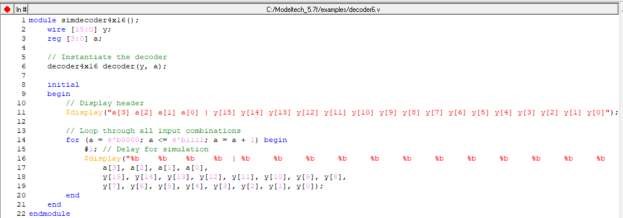
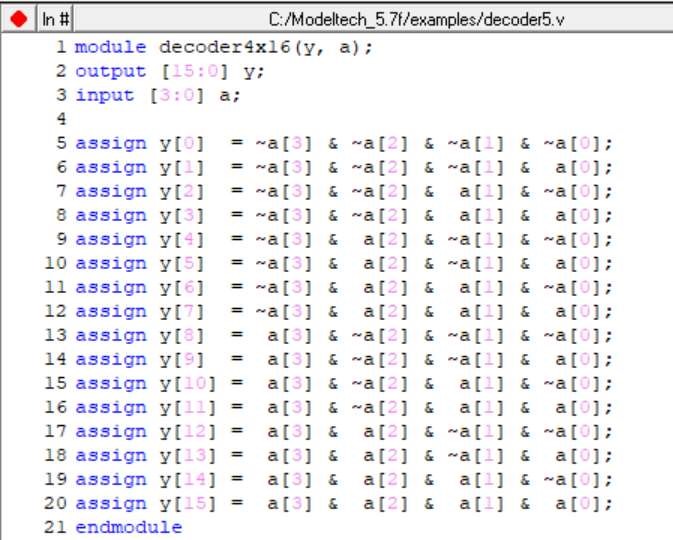
Description automatically generated



**TASK 3:**

Write a Verilog code for 4x16 Decoder using Dataflow Level modeling.

**Code:**



**Output:**

A diagram of a computer program

Description automatically generated with medium confidence

**Remarks:**

1. **Definition**: A decoder is a combinational circuit that converts binary input data into a specific output line, with only one output line active (logic 1) at a time.
2. **Purpose**: Decoders are commonly used in applications such as memory address decoding, data routing, and enabling specific devices in digital systems.
3. **Types**:
   * **2x4 Decoder**: Converts 2 input lines into 4 output lines.
   * **3x8 Decoder**: Converts 3 input lines into 8 output lines.
   * **4x16 Decoder**: Converts 4 input lines into 16 output lines.  Larger decoders, like 5x32, can also be constructed.
4. **Working Principle**: For an n-input decoder, exactly one of the 2^n output lines is active based on the binary input combination.